SWITCHED-CAPACITOR SAMPLE/HOLD HAVING REDUCED AMPLIFIER SLEW-RATE AND SETTLING TIME REQUIREMENTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to analog signal sampling circuits, and more specifically, to a switched-capacitor sample/hold having reduced amplifier slew-rate and settling time requirements.

2. Background of the Invention

Switched-capacitor sample/hold circuits are in common use today. Integrated circuits such as analog-to-digital (A/D) converters as well as voltage-to-frequency (V/F) converters, switched capacitor filters and other analog signal processing components often incorporate switched-capacitor circuits and in particular switched-capacitor sample/hold circuits to provide sampling and filtering circuits with controllable gain and circuit performance.

The simplest form of sample/hold circuit utilizes a single capacitor and a switch that samples the input signal onto the capacitor for a fixed interval. The capacitor is followed by a buffer amplifier that isolates subsequent stages. Improved

switched-capacitor sample/hold circuits alternate the position of a single capacitor between an input signal terminal and a feedback position in the follower amplifier, providing a sampled state that is isolated from the input and has low droop in the hold phase. However, the simple alternating position sample/hold circuit requires that the amplifier transition from a zero state to a full value corresponding to the sampled signal at each sampling interval.

Improved versions of the simple alternating position sample/hold circuit have been developed that use a secondary holding capacitor to hold the previous output value at the amplifier during the sample state, but for high level input signals at input frequencies approaching half of the sampling rate (i.e., the Nyquist rate), the amplifier still must transition significantly from the sample state to the hold state, as the previous value has changed significantly from the last sample. The requirement on the amplifier to respond to steps in output voltage in all of the above-described circuits sets a minimum slew rate and settling time requirement for a particular accuracy in the sample/hold circuit. The slew rate and setting time of the amplifier are a source of error in the switched-capacitor sample/hold circuit. The slew rate and settling time are cost drivers for the amplifier, and within an

integrated circuit can mean increased area and power dissipation and/or increased voltage requirements.

Another source of error in switched-capacitor circuits in general, and switched-capacitor sample/hold circuits in particular, is error due to charge injection. Charge injection occurs when the control input of a switch that couples an analog signal to the sampling or holding capacitor transitions and charge is transferred via capacitive coupling from the control input of the switch (typically the gate of a MOSFET) to the capacitor.

Non-linearity error is particularly pervasive in the input switches of sample/hold circuits, as the switch control signals are typically logic signals and as the sampled input voltage increases, the difference between the gate-to-source voltage of the switch transistors over the threshold voltage effectively decreases in a manner that is dependent on the input signal and thereby introduces non-linearities.

Therefore, it would be desirable to provide a sample/hold circuit having reduced amplifier settling time and slew-rate requirements and reduced error resulting from amplifier settling time and slew-rate. It would further be desirable to provide

such sample/hold circuit that has reduced susceptibility to error due to charge injection and improved linearity.

SUMMARY OF THE INVENTION

The above objective of providing a switched-capacitor sample/hold circuit having a reduced amplifier slew rate and settling time requirement and reduced error due to amplifier slew rate and settling time is provided in a new switched-capacitor sample/hold circuit and method of operation of a sample/hold circuit. The above objectives of reducing error due to charge injection and improving linearity is provided in a differential embodiment of the circuit and method of the present invention.

The new switched-capacitor sample/hold circuit includes two capacitors, both of which are alternatively and mutually-exclusively placed in an input sampling position and an amplifier feedback hold position, providing a double sampling of the input signal that reduces the magnitude of transitions on the output of the sample/hold amplifier.

The differential embodiment of the new sample/hold circuit uses four capacitors and a fully differential buffer amplifier that includes a differential input and a differential output. The above-described double-sampled switched-capacitor circuit is effectively duplicated for each negative feedback output-input

pair of the differential amplifier (e.g., one circuit is connected to the inverting input and the non-inverted output and the other circuit is connected to the non-inverting input and the inverted output). The two double-sampled switched-capacitor circuits are referenced to each other rather than a ground node, providing fully differential operation that cancels error due to charge injection to the degree of symmetry of the charge-injection magnitude (e.g., the matching of the input switching transistor gate-drain capacitances C_{gd}).

The foregoing and other objectives, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiment of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram depicting a sample/hold circuit in accordance with an embodiment of the present invention.

Figure 2 is a pictorial diagram depicting signals within a sample/hold circuit in accordance with an embodiment of the present invention shown in contrast with signals for a typical sample/hold circuit.

Figure 3 is a schematic diagram depicting a sample/hold circuit in accordance with another embodiment of the present invention.

Figure 4A is a schematic diagram depicting a bootstrap clock circuit as may be used to implement bootstrap clock circuits **31A-H** of **Figure 3**.

Figure 4B is a signal diagram showing the relationship of signals within the bootstrap clock circuit of **Figure 4A**.

Figure 5A is a schematic diagram depicting a clock driver circuit for use with the sample/hold circuit of **Figure 3**.

Figure 5B is a timing diagram showing the relationship of clock phases of the clock driver circuit of **Figure 4A**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the figures, and in particular to **Figure 1**, a sample/hold circuit in accordance with an embodiment of the invention is depicted. An input voltage **Vin** is alternatively applied to a first capacitor **C11** or a second capacitor **C13** via switches **S11** and **S12** to sample an input signal. When capacitor **C11** is selected for sampling, switch **S17** is closed, grounding a second terminal of capacitor **C11**, similarly switch **S18** grounds a second terminal of capacitor **C13**, when capacitor **C13** is selected for sampling. The capacitor (**C11** or **C13**) that is not selected for sampling is connected via switches **S13** and **S15** (for **C11**) or switches **S14** and **S16** (for **C13**) in the feedback path of an amplifier **A11**, which provides a sampled output **Vout**. The control signals for switches **S11-S18** are provided by buffer **B11** and inverter **I11** so that two complementary phases of the sampling clock signal are provided for selecting the alternate states required for switches **S11-S18**. The circuit of **Figure 1** is a simplified circuit provided for illustration, and actual implementations will generally use more complex switching clock phase arrangements so that overlapping switch states are not generated, as will be described below in more detailed embodiments of the present invention.

With further reference to **Figure 2**, operational advantages of the sample/hold circuit of the present invention are illustrated. As can be seen from the diagram at the top of the figure, amplifier **A11** output **Vout** has a step characteristic that follows the shape of input signal **Vin**. Note that the **Vout** signal is delayed by one-half of the sample clock period, as the sampled value is not transferred to the amplifier **A11** output until the alternate state of the sample clock. In contrast, a sampled waveform of output signal **Vprior** of a typical sample/hold circuit is depicted in the lower sampling diagram. Note that the sampled waveform is also delayed by one-half of the sampling interval, but contains half as many steps, as the input sampled value is only transferred to the amplifier once per sample clock period. The result is that transitions of the sampled waveform such as transition **23** are larger than the transitions of the **Vout** signal of the present invention (such as transition **21**) for signals approaching the Nyquist frequency (i.e., ½ of the sample clock frequency) as depicted in the portion of the input waveform in the center of the diagram near transitions **21** and **23**. In general, the largest transitions in a sample/hold circuit output, and thus the greatest demands on the amplifier are produced for signals closest to the Nyquist frequency, as lower-frequency input signals change more slowly

and thus the variation in the output signal is spread over more samples.

Therefore, the sample/hold circuit of the present invention has relaxed slew rate and settling time requirements for amplifier **11** for a given allowable sampling error, and/or a lower sampling error for a given amplifier performance. Therefore, the circuit of **Figure 1** can provide improved performance for a particular design, or provide a lower-power or circuit size design for a predetermined sample/hold performance level. Also, it should be noted that while the doubled number of steps shown in signal **Vout** is due to a double-sampled operation within the sample/hold circuit of the present invention, only half of the steps are actually used in further conversion or other operations. The output signal taken during either phase of sample clock, but not both. In effect, the internal update rate of the amplifier is doubled, reducing the size of transitions the amplifier output must make, while the actual sample rate of the sample/hold remains the same.

Referring now to **Figure 3**, a sample/hold circuit in accordance with an embodiment of the present invention is depicted. The circuit of **Figure 3**, includes several improvements and implementation details not shown in the circuit of **Figure 1**.

Bootstrap clock circuits **31A** are provided with multiple non-overlapping phases generated by a clock phase generator circuit and control the gates of the switch transistors with a source-terminal dependent level to improve linearity of the sample/hold circuit. Also, the sample/hold circuit of **Figure 3** is a fully differential circuit, which further reduces charge injection error and other errors in the sample/hold circuit, as the differential design provides protection from common-mode noise and cancels charge injection error, which is a common-mode error for the circuit configuration shown. (The switch transistors are of the same type and switched by the same clock phase/voltage levels, so the charge transfer has the same polarity and a magnitude that differs only due to differences between the C_{gs} of the switch transistors).

Switch transistors **N31** and **N32** control placement of capacitor **C31** in the input sample position, while switch transistors **N33** and **N34** control placement of capacitor **C31** in a feedback path of amplifier **A31** (in this case, the negative feedback path between the non-inverted output and the inverting input of amplifier **A31**). Similarly capacitor **C33**, which samples in alternation with capacitor **C31** in a manner similar to the operation of the circuit of Figure 1, is placed in the input sample position by activation of switch transistors **N35** and **N36**,

while transistors **N38** and **N37** control placement in the above-described feedback path of amplifier **A31**. Bootstrap clock circuits **31A-B** provide control of input switch transistors **N31** and **N35**, so that linearity is improved as described below, and bootstrap clock circuits **31E-F**, provide control of switch transistors **N34** and **N38**, also reducing non-linearity resulting from differences between steps in the output signal of amplifier **A31**.

At the bottom of **Figure 3**, a circuit identical to that described above is coupled to the non-inverting input and the inverted output terminals of amplifier **A31**, providing the fully differential sample/hold circuit of the present embodiment. Switch transistors **N131** and **N132** control placement of capacitor **C37** in the input sample position, while switch transistors **N133** and **N134** control placement of capacitor **C37** in the other feedback path of amplifier **A31** (the negative feedback path between the inverted output and the non-inverting input of amplifier **A31**). Similarly capacitor **C35**, which samples in alternation with capacitor **C37**, is placed in the input sample position by activation of switch transistors **N135** and **N136**, while transistors **N138** and **N137** control placement in the above-described other feedback path of amplifier **A31**. Bootstrap clock circuits **31C-D** provide control of input switch transistors **N131**

and **N135**, and bootstrap clock circuits **31G-H**, provide control of switch transistors **N134** and **N138**.

Rather than referring the input signal to ground as in the non-differential circuit of Figure 1, in the embodiment of Figure 3, a common-mode reference signal **Vcm** is supplied. Switch transistors **N32**, **N36**, **N132** and **N136** couple their respective capacitors as described above to this common-mode reference, rather than ground. Also, Switch transistors **N39** and **N40**, are activated to further reduce any differences between the common-mode voltage as applied to the common-mode terminal of capacitors **C31** and **C37** (by transistor **N39**) and capacitors **C33** and **C35** (by transistor **N40**), when the associated capacitors are selected for sampling the input.

The circuit of **Figure 3** thus provides a highly accurate sample/hold circuit that has improved accuracy in particular for frequencies near the Nyquist frequency. The circuit is capable of sampling an input signal frequency at 100Mhz at a 60Ms/s sampling rage with a spurious-free dynamic range (SFDR) greater than 80dB. At low input signal frequencies, SFDR performance rises to greater than 90dB.

Referring now to **Figure 4A**, a bootstrap clock circuit **31** as may be used to implement bootstrap clock circuits **31A-H** of **Figure 3** is depicted. Referring also to **Figure 4B**, signals within the circuit of **Figure 4A** are depicted for illustration of operation. **Φd** is the d-phase input as indicated for each bootstrap circuit **31A-H** and **Φdp** is a complement (inverse) of the **Φd** clock signal. **Φc** is the c-phase clock input, also as indicated for each bootstrap circuit. The c-phase clock signal is the clock signal for the opposing sampling phase, used because it is valid for a window within the period while the d-phase clock signal is deasserted. Note that the **Φ1d** signal is used with the **Φ2c** signal and the **Φ1c** signal is used with the **Φ2d** signal in the circuit of **Figure 3**.

The gate of an external transistor (e.g., transistor **N31** as shown) is controlled by bootstrap clock circuit **31** in conformity with the above-mentioned clock inputs and with a sensed source voltage of the external transistor. Prior to assertion of the c-phase clock signal, capacitor **C41** is charged to **Vdd** through transistor **N51** and transistor **N52** when the d-phase clock signal is deasserted. Transistor **N52** which couples the terminal of capacitor **C41** opposite transistor **N52** to ground until the c-phase clock signal is asserted, at which time capacitor **C41** is

fully charged to **Vdd**. A transmission gate formed by transistors **N53** and **P52** is enabled by the d-phase clock and couples the source of the external transistor to a first terminal of capacitor **C41**, raising the second terminal of capacitor **C41** to a signal-dependent level (**Vdd+Vs**). Simultaneously, the raised voltage level is applied to the gate of the external transistor through transistor **P51** and when the d-phase clock is deasserted, transistors **N53**, **P52** and **P51** are turned off and the gate of the external transistor is left floating. At the end of the phase-c signal, a transistor **N54** completely turns off the gate of the external transistor. The bootstrap circuit depicted applies a voltage-dependent gate control signal for switching that maintains switching transistor Vgs (on) at a constant level and thus improves linearity of the sample/hold circuit.

Referring now to **Figure 5A**, a clock generator circuit is depicted for providing the clock signals used in the circuits of Figures 3 and 4. Referring further to **Figure 5B**, the timing relationship of the above-mentioned clock signals is shown. Buffers **B51-B54** forms a buffer chain that receives the sample clock input and generate four phases of a sampling clock for a first sampling phase, consecutively delayed by the delays of the buffer chain. Inverter **I51** inverts the c-phase clock and delays it by the same delay as provided by buffer **B54**, providing a

complementary d-phase signal. Buffers **B55-B58** form a second buffer chain providing four clock phases for a second sampling phase and inverter **I52** provides an inverted version of the second d-phase signal. The timing relationships of the clock generator signals are as depicted in **Figure 5B**.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.